NT5AD512M16C4-JR

Commercial DDR4 Memory Solution

Technical Datasheet

Source Memory Chips (SMC) provides technical reference documentation for memory products used in industrial, networking, embedded and long-life electronic applications.

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1. Product Overview

NT5AD512M16C4-JR is an 8Gb DDR4 SDRAM component from Nanya Technology. The device is organized as 512M x16, supports a data rate of 3200 MT/s, and is supplied in a 96-ball TFBGA package for compact board-level memory designs.

The JR ordering code identifies the DDR4-3200 speed grade with CL-tRCD-tRP of 22-22-22. The device uses 1.2V VDD and VDDQ rails with a 2.5V VPP activation supply, and the commercial-grade operating range is 0 C to 95 C case temperature.

Parameter	Specification
Manufacturer	Nanya Technology
Part Number	NT5AD512M16C4-JR
Memory Type	DDR4 SDRAM
Density / Organization	8Gb / 512M x16
Data Rate	3200 MT/s
Package	96-ball TFBGA
Grade / Temperature	Commercial / 0 C to 95 C
Current Portfolio Status	Available

Figure 1. NT5AD512M16C4-JR key product identifiers

Key Takeaways

- 8Gb DDR4 SDRAM with a native x16 data interface.
- DDR4-3200 speed grade in a compact 96-ball TFBGA package.
- Commercial-temperature product; it must not be represented as an industrial-grade suffix.

2. Ordering Information

The complete ordering code should be used during engineering qualification and procurement. Each segment of NT5AD512M16C4-JR identifies the manufacturer family, DDR generation, power interface, organization, device revision, package code, and speed grade.

NT	5A	D	512M16	C	4	JR
Nanya component	DDR4 SDRAM	1.2V / 1.2V / 2.5V	8Gb, x16 organization	3rd device version	96-ball TFBGA	3200 MT/s, 22-22-22

Code Segment	Meaning for NT5AD512M16C4-JR
NT	Nanya component
5A	DDR4 SDRAM
D	1.2V / 1.2V / 2.5V
512M16	8Gb, x16 organization
C	3rd device version
4	96-ball TFBGA
JR	3200 MT/s, 22-22-22

Design Note

- JR is the speed suffix: DDR4-3200 with 22-22-22 primary timing designation.
- No trailing grade letter means commercial grade. JRI, JRT and JRU are different ordering codes and must not be substituted without validation.
- Verify the full device marking, date code and traceability record before production approval.

3. NT5AD512M16C4-JR Key Specifications

NT5AD512M16C4-JR is an 8Gb memory component manufactured by Nanya Technology and organized as 512M x16. The model-specific specifications below define the baseline for component selection, controller configuration, PCB planning and thermal qualification.

Specification	NT5AD512M16C4-JR Value	Engineering Relevance
Density	8Gb	Total component memory capacity
Organization	512M x16	16-bit component interface
Memory Technology	DDR4 SDRAM	Controller and platform compatibility
Maximum Data Rate	3200 MT/s	Rated transfer speed of the -JR bin
Primary Speed Grade	22-22-22	CL-tRCD-tRP designation
Supply Rails	VDD 1.2V, VDDQ 1.2V, VPP 2.5V	Device power requirements
Package	96-ball TFBGA, 7.50 x 13.00 mm	PCB footprint and assembly requirement
Grade / Status	Commercial, 0 C to 95 C / Available	Qualified environment and portfolio status

NT5AD512M16C4-JR Device Summary

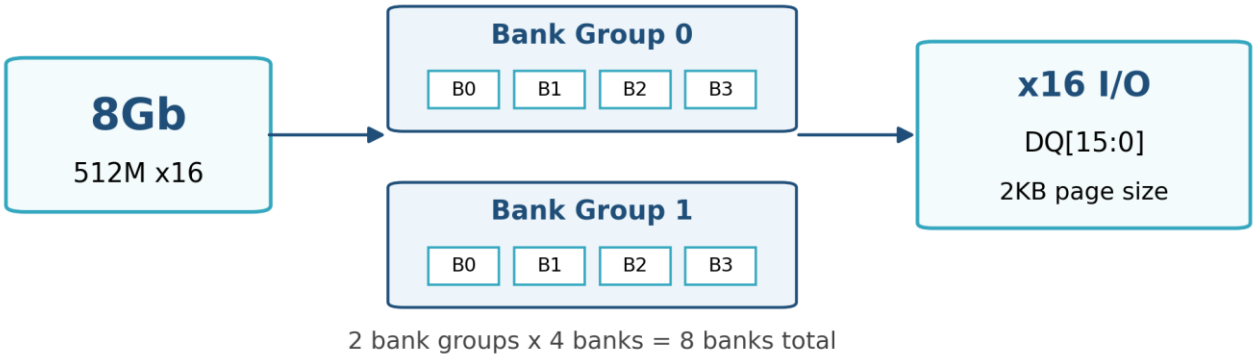
- Nanya Technology 8Gb component with a native x16 interface.
- Maximum transfer rate of 3200 MT/s with the -JR 22-22-22 speed grade.
- 96-ball TFBGA package with 1.2V VDD/VDDQ and 2.5V VPP supply rails.
- Commercial operating range of 0 C to 95 C; the exact -JR suffix must be retained.

Capacity note: 8Gb is the component density; the physical organization of NT5AD512M16C4-JR remains 512M x16.

4. Memory Organization

NT5AD512M16C4-JR is organized as 512M locations by 16 data bits. The x16 implementation uses two bank groups, with four banks in each group, for a total of eight banks. This organization supports parallel bank activity while maintaining a compact 16-bit board interface.

Figure 2. NT5AD512M16C4-JR logical organization



Organization Parameter	Device Value
Bank Groups	2 (BG0)
Banks per Group	4 (BA[1:0])
Total Banks	8
Row Address	A[15:0]
Column Address	1K columns, A[9:0]
Page Size	2KB
Refresh Cycle Time	tRFC = 350 ns

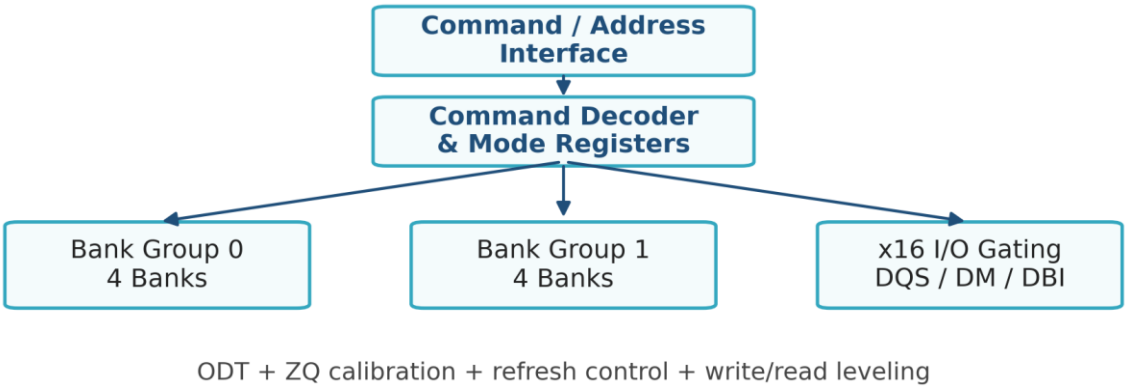
Implementation Notes

- The x16 interface uses separate upper and lower byte data strobes and mask/DBI functions.
- Controller address mapping must match the x16 bank-group and row/column organization.
- Refresh scheduling changes above 85 C and is detailed in the operating-conditions section.

5. NT5AD512M16C4-JR Internal Architecture

NT5AD512M16C4-JR is organized as a 512M x16, 8Gb device. Its internal path coordinates command/address decoding, two bank groups with four banks per group, and an x16 data interface divided into upper and lower byte lanes synchronized by DQS pairs.

Figure 3. Simplified functional architecture of NT5AD512M16C4-JR



NT5AD512M16C4-JR Design Area	Device-Specific Description
Memory organization	512M x16; 8Gb total density
Bank structure	2 bank groups with 4 banks per group
Data interface	x16 I/O with upper and lower byte lanes and DQS pairs
Command path	Differential clock input with command/address decoding
Calibration / training	ODT, ZQ calibration and controller-supported read/write leveling
Refresh behavior	Normal refresh through 85 C; higher refresh frequency above 85 C

NT5AD512M16C4-JR Integration Focus
- Configure the controller for the device's x16 bank-group organization.
- Match DQ signals to the corresponding DQS pair within each byte lane.
- Use platform-supported leveling and VREFDQ training during initialization.
- Apply the complete Nanya timing and mode-register requirements during validation.

6. Electrical Characteristics

NT5AD512M16C4-JR uses separate core, I/O and activation supply rails. VDD and VDDQ are nominally 1.2V and should track each other; VDDQ must remain less than or equal to VDD. VPP is the 2.5V activation supply.

Figure 4. Recommended supply rails

Rail	Recommended Min	Typical	Recommended Max	Absolute Max
VDD	1.14V	1.20V	1.26V	1.50V
VDDQ	1.14V	1.20V	1.26V	1.50V
VPP	2.375V	2.50V	2.75V	3.00V

Additional Rating	Minimum	Maximum
Voltage on other pins vs. VSS	-0.3V	1.5V
Storage temperature	-55 C	100 C

Power-Integrity Notes

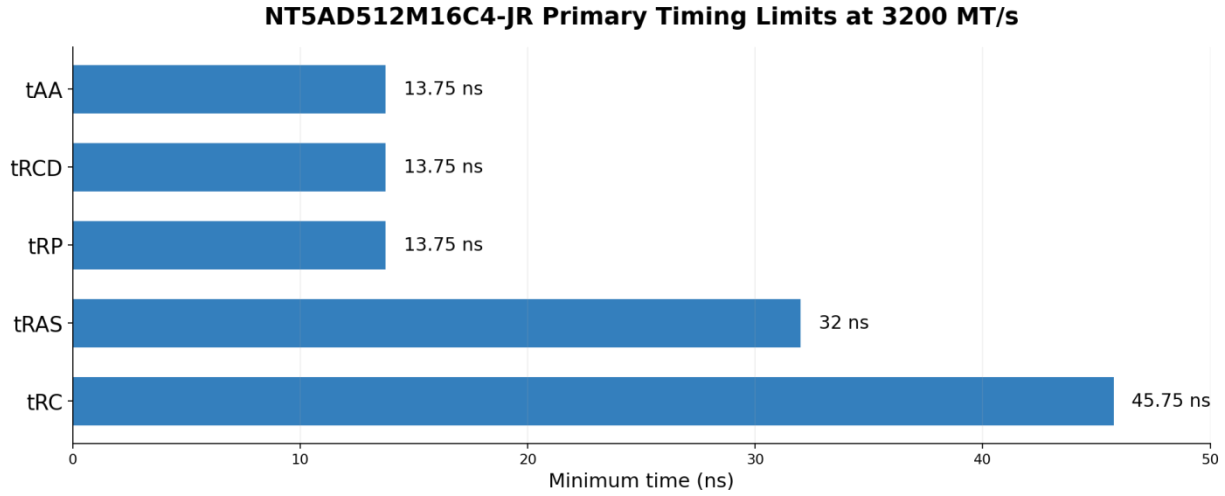
- Keep VDD and VDDQ within 300mV of each other at all times.
- Use local high-frequency decoupling and continuous return paths close to the 96-ball package.
- Absolute maximum ratings are stress limits, not normal operating conditions.

7. NT5AD512M16C4-JR Timing and Performance

NT5AD512M16C4-JR supports a maximum data rate of 3200 MT/s under the -JR speed grade. At this operating point, the external clock frequency is 1600 MHz and the primary timing designation is 22-22-22. Final controller settings must satisfy the latest Nanya operating and mode-register requirements.

NT5AD512M16C4-JR Timing Parameter	Symbol	Minimum Requirement
Average clock period at 1600 MHz	tCK(avg)	0.625 ns
READ command to first data	tAA	13.75 ns
ACTIVATE to READ/WRITE	tRCD	13.75 ns
PRECHARGE command period	tRP	13.75 ns
ACTIVATE to PRECHARGE	tRAS	32.00 ns
ACTIVATE to ACTIVATE/REFRESH	tRC	45.75 ns

Figure 5. NT5AD512M16C4-JR primary timing limits at 3200 MT/s



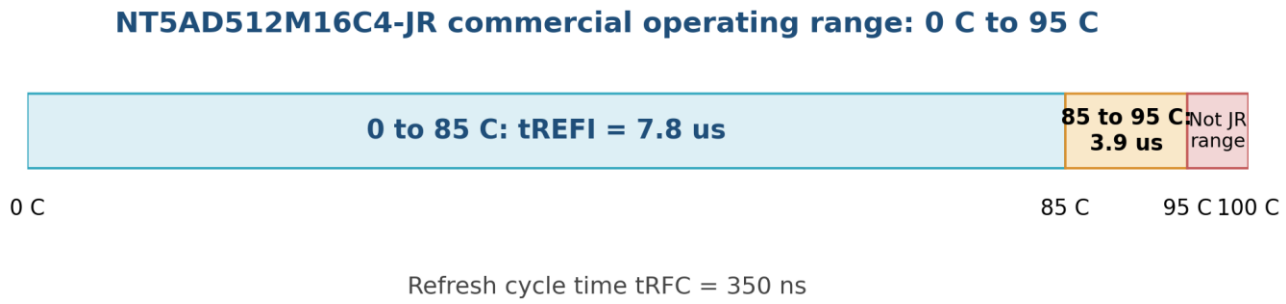
NT5AD512M16C4-JR Interface Performance

- Maximum supported data rate: 3200 MT/s; external clock frequency: 1600 MHz.
- Theoretical peak x16 interface bandwidth: 6.4 GB/s.
- The 6.4 GB/s value is a calculated interface maximum, not guaranteed sustained throughput.
- Actual performance depends on controller efficiency, refresh activity, access patterns and board-level signal integrity.

8. Operating Conditions and Refresh

NT5AD512M16C4-JR is the commercial-grade member of the C-die x16 family and is specified for a case-temperature range of 0 C to 95 C. The device requires more frequent refresh above 85 C to preserve data-retention margin.

Figure 6. Temperature range and refresh interval



Case Temperature Region	Required tREFI	Qualification Meaning
0 C to 85 C	7.8 us	Normal commercial operating region
Above 85 C to 95 C	3.9 us	High-temperature refresh region
Above 95 C	Not specified for -JR	Use a correctly graded ordering code

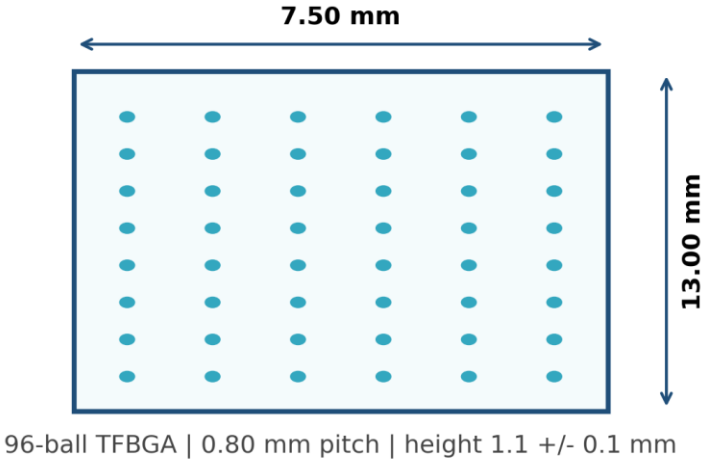
Operating Guidance

- Monitor worst-case case temperature at the package center/top surface during qualification.
- Program the memory controller to apply the appropriate refresh interval across the full thermal envelope.
- Do not describe or qualify the -JR suffix as an industrial-temperature component.

9. NT5AD512M16C4-JR Package Integration

NT5AD512M16C4-JR is supplied in a 96-ball TFBGA package for its x16 interface and operation up to 3200 MT/s. The 7.50 x 13.00 mm body and 0.80 mm ball pitch define the PCB footprint; the final land pattern and ball assignment must be verified against the latest Nanya package drawing.

Figure 7. NT5AD512M16C4-JR 96-ball TFBGA package overview



Package Parameter	NT5AD512M16C4-JR Requirement
Package Type	96-ball TFBGA
Body Dimensions	7.50 x 13.00 mm
Ball Pitch	0.80 mm
Nominal Height	1.1 +/- 0.1 mm
Device Interface	x16, up to 3200 MT/s
Supply Connections	VDD, VDDQ and VPP
Temperature Grade	Commercial, 0 C to 95 C

NT5AD512M16C4-JR PCB Integration Checklist

- Create the footprint from the official Nanya package drawing and ball map.
- Route CK/CK# as a matched differential pair and match DQ signals to each DQS byte lane.
- Place local decoupling close to the VDD, VDDQ and VPP supply balls with continuous return paths.
- Validate signal integrity, power integrity, timing margin and assembly quality before production release.

10. Qualification and Application Fit

The combination of 8Gb density, x16 organization and DDR4-3200 performance makes NT5AD512M16C4-JR suitable for commercial-temperature systems that need a compact component-level memory interface. Typical design targets include embedded computing, networking equipment, consumer platforms and office/enterprise electronics operated within the specified thermal range.

Figure 8. Recommended qualification sequence

Review Area	Required Check
Part Identity	Full NT5AD512M16C4-JR marking and suffix
Controller Support	x16 DDR4-3200 timing and training capability
Power Design	1.2V VDD/VDDQ and 2.5V VPP sequencing and margin
PCB Channel	Impedance, byte-lane matching, ODT and ZQ implementation
Thermal Validation	0 C to 95 C case-temperature compliance
Supply Chain	Date code, traceability, lifecycle and approved source

Application Boundary

- Application examples describe design fit, not automatic qualification for every platform.
- Medical, automotive, safety-critical or wide-temperature use requires the correct grade, manufacturer approval and system-specific validation.
- The commercial -JR part should remain the exact focus of procurement documents and BOM records.

11. Conclusion

NT5AD512M16C4-JR is a Nanya 8Gb DDR4 SDRAM component organized as 512M x16 and rated for DDR4-3200 operation. Its 96-ball TFBGA package, 1.2V core and I/O rails, 2.5V activation rail, and commercial 0 C to 95 C operating range define the key boundaries for system integration.

For a reliable implementation, the full ordering code must be retained, the 22-22-22 speed grade must be configured correctly, refresh must be adjusted above 85 C, and the board must be validated for DDR4-3200 power and signal integrity.

Final Parameter	Specification
Manufacturer	Nanya Technology
Part Number	NT5AD512M16C4-JR
Density / Organization	8Gb / 512M x16
Rated Speed	DDR4-3200, 22-22-22
Supply	1.2V VDD, 1.2V VDDQ, 2.5V VPP
Package	96-ball TFBGA, 7.50 x 13.00 mm
Temperature / Grade	0 C to 95 C / Commercial
Portfolio Status	Available

Final Key Takeaways

- Exact-model technical summary centered on NT5AD512M16C4-JR.
- Commercial DDR4-3200 x16 solution with an 8Gb memory array.
- Final production use requires the latest Nanya datasheet, controller documentation and completed platform qualification.

Reference basis: Nanya Commercial and Industrial DDR4 8Gb SDRAM C-Die component datasheet, Version 2.7 (03/2024); Nanya Standard DRAM Part Numbering Guide (2025); Nanya product listing for NT5AD512M16C4-JR, Datasheet Rev. 2.8, updated 2026-01-13. This SMC document is a technical reference summary and does not replace manufacturer-controlled documentation.